UNITED STATES PATENT APPLICATION

FOR

METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION IN A GRAPHICS CONTROLLER

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Attorney's Docket No: 3935P012

METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION IN A GRAPHICS CONTROLLER

BACKGROUND OF THE INVENTION

Field of the Invention

[01] This invention relates generally to the fields of graphics control and power management and more specifically to managing power consumption in a graphics controller subsystem.

Description of the Related Art

[02] Computer systems have been implemented for years as desktop systems utilizing monitors. With the advent of laptop systems and of increasing awareness of power consumption in general, some moves have been made to cause central processing units and monitors to conserve power. However, other portions of a computer may also be used to conserve power. Furthermore, in laptops in particular, conserving battery power may prove to be of great importance to potential users. While companies such as AMD and Intel have been providing power sensitive central processing units, no power sensitive graphics controllers are currently available. Given that power-intensive nature of graphics controllers, taking advantage of potential power savings therein may enhance the value of systems using graphics controllers.

SUMMARY OF THE INVENTION

[03] The invention in one embodiment is a method of managing power in a graphics controller. The method includes receiving a change indication related to a system power supply. The method also includes adjusting a first clock or adjusting a set of clocks including a first clock. The method further includes adjusting a controller power supply voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[04] The present invention is illustrated by way of example and not limitation in the accompanying figures.

[05] Figure 1 illustrates a block diagram of an embodiment of a system.

[06] Figure 2 illustrates an alternate embodiment of a system.

[07] Figure 3A illustrates an embodiment of a method of reducing power consumption.

[08] Figure 3B illustrates an embodiment of a method of restoring normal power usage.

[09] Figure 4 illustrates an embodiment of a graphics controller.

[10] Figure 5 illustrates one embodiment of a graphics subsystem which may incorporate the invention.

[11] Figure 6 illustrates one embodiment of a system which may incorporate the graphics subsystem which may incorporate the invention.

[12] Figure 7 illustrates another alternate embodiment of a system.

DETAILED DESCRIPTION

[13] A method and apparatus for reducing power consumption in a graphics controller is described. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the invention. It will be apparent, however, to one skilled in the art that the invention can be practiced without these specific details. In other instances, structures and devices are shown in block diagram form in order to avoid obscuring the invention.

[14] Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment, nor are embodiments mutually exclusive.

[15] The method and apparatus incorporate power management into a graphics controller or processor. In one embodiment, a programmable voltage regulator is used to supply power to the graphics controller, such that the graphics controller may adjust the voltage of the regulator when a low-power condition (such as a switch from AC to battery power in a laptop computer) is detected. Additionally, in one embodiment, low-power conditions are detected by inserting a software routine into the operating system which intercepts the operating system power change signal and relays an indication of a power

change to the graphics controller. Furthermore, in one embodiment, a video clock may be set to a lower clock rate for power savings, as the video clock often affects the power consumption of a monitor and may also affect the power consumption of the graphics controller due to processing demands. Moreover, in one embodiment, a memory clock may be set to a lower rate, thus slowing down memory accesses and thereby conserving power. In particular, in one embodiment, the memory clock rate is determined based on the state of the graphics controller. Additionally, a color lookup table and other portions of a graphics controller may be disabled or transitioned to a low-power mode to reduce power consumption. Furthermore, in one embodiment, the graphics controller may signal to the surrounding system that various other power saving measures, such as lowering a monitor supply voltage or turning down a monitor brightness may be appropriate.

[16] The invention in one embodiment is a method of managing power in a graphics controller. The method includes receiving a change indication related to a system power supply. The method also includes adjusting a first clock or a set of clocks. The method further includes adjusting a controller power supply voltage. The method may also include powering down or otherwise disabling one or more portions of circuitry.

[17] Turning to the drawings, Figure 1 illustrates a block diagram of an embodiment of a system. Processor 110 may interact with the graphics controller 140 either directly or through VGA BIOS 130. Graphics controller 140

is supplied with power by power regulator 150, which receives its power from the system power supply (not shown). Power regulator 150 also may receive a signal from graphics controller 140 which may trigger a change in the voltage at which power is supplied to graphics controller 140. In one embodiment, power regulator 150 normally supplies power at 2.5 V, and supplies power at 2.0 V under power saving conditions indicated by the signal from graphics controller 140. In an alternate embodiment, power regulator 150 normally supplies power at 3.3 V, and supplies power at 2.5V under power saving conditions indicated by the signal from graphics controller 140. In one embodiment, the voltage regulator is a model VT101, VT102 or VT103, each of which is available from the Volterra corporation.

[18] Coupled to graphics controller 140 is also LCD 170 which is a liquid crystal display. Graphics controller 140 controls some aspects of the operation of LCD 170, and the video clock used by LCD 170 may be supplied by graphics controller 140. Note that the video clock used by LCD 170 may be set to a lower clock rate (frequency) than the clock rate for graphics controller 140. Also coupled to processor 110 and LCD 170 is chipset 180, which controls other aspects of operation of LCD 170. Chipset 180 may control the supply voltage and brightness of LCD 170 for example. In one embodiment, chipset 180 and graphics controller 140 are coupled directly, allowing for communication directly between the graphics controller 140 and the chipset 180. Note that chipset 180 and other components of Figure 1 may take on a variety of forms, such as a

single integrated circuit (IC) implementation, multiple IC implementation, or discrete implementations within the spirit and scope of the invention.

[19] Figure 2 illustrates an alternate embodiment of a system. Note that the embodiments illustrated in Figures 1 and 2 may be similar or the same, depending on implementation by one skilled in the art. Operating system 210 is coupled to or includes driver 220. Driver 220 communicates with graphics controller 240 either directly or through VGA BIOS 230, thus allowing operating system 210 to communicate with graphics controller 240. Graphics controller 240 receives its power from voltage regulator 250 through Vcc 243, and controls the power output of voltage regulator 250 through Vcc control 247. Graphics controller is also coupled to VRAM 260 through at least MCLK 245, a clock signal, and potentially other signals or buses as appropriate. Furthermore, graphics controller 240 is coupled to LCD 270 through at least VCLK 273 and VCLK control 276. VCLK 273 is a clock signal and VCLK control 276 is a control signal which indicates which clock frequency is in use. LCD 270 is also coupled to chipset 280 through at least brightness 284 and Vcc 287. Vcc 287 supplies power to the LCD 270 (with chipset 280 functioning as a power supply or regulator) and brightness 284 indicates what brightness level the LCD 270 should use to operate. Chipset 280 is also coupled to the operating system 210, possibly through a separate BIOS for example. Note that the VCLK control 276 signal may not be included in some implementations or embodiments, as the VCLK may shift without a corresponding control signal. Furthermore, note that

component 290 includes both the graphics controller 240 and the memory (VRAM 260), as those two portions of the system may easily be integrated to form a single component.

[20] Figure 3A illustrates an embodiment of a method of reducing power consumption. At block 310, a change in power supply is detected, such as by an operating system which receives a signal from underlying system power management hardware. Additionally, this signal is, in one embodiment, intercepted by a driver for a graphics controller, which provides an indication of the change to the graphics controller. At block 320, the graphics or VGA BIOS is informed of a switch in power supply modes by the graphics controller. This process of informing may also include a request for a set of preprogrammed clock rate values which are stored in the VGA BIOS and programmed by the operating system in one embodiment. At block 330, the video clock for the LCD (a first clock for example) is adjusted to a lower rate or frequency. At block 340, a graphics controller power supply voltage is programmed for a lower voltage level or other wise adjusted. At block 350, the system is notified that changing brightness of the monitor may be appropriate for power saving purposes. At block 360, a set of available clock rates is returned from the VGA BIOS. At block 370, the state of the graphics controller is checked, such as determining whether a 3D engine or a 2D engine is active. Based on the state of the graphics controller, at block 380, an available clock rate from the set of clock rates is chosen for a memory clock (a second clock for example) and the memory clock

is set to run at the available clock rate. It will be appreciated that the memory clock may effectively remain unchanged (at the same clock rate) as appropriate due to the type of graphics activity occurring in the system. At block 390, again based on the state of the graphics controller, the CLUT (color lookup table) is disabled if possible, thus further saving power.

[21] Figure 3B illustrates an embodiment of a method of restoring normal power usage. At block 315, a change in the underlying power system is detected, such as by the operating system when a laptop switches to AC power. Similarly, this signal is intercepted and relayed to the graphics controller. At block 325, the VGA BIOS is informed of the switch by the graphics controller to full power mode. At block 335, the video clock is adjusted to an optimal speed independent of power considerations. At block 345, the graphics controller power supply voltage is programmed for a higher voltage level. At block 355, the system is notified that increasing brightness or other operating parameters of a monitor may be appropriate. At block 375, a memory clock is set to a higher level, either as determined within the graphics controller or from a set of clock rates provided by the VGA BIOS. At block 385, the CLUT is enabled, thus taking advantage of power to enhance performance.

[22] Figure 4 illustrates an embodiment of a graphics controller. Graphics controller 400 includes the various components illustrated. 2D engine 410 may be used for rendering two-dimensional graphics. 3D engine 420 may be used for rendering three-dimensional graphics. Video engine 425 may be

used to process motion video. CLUT 430 is a color lookup table suitable for quickly translating stored color values for rendering purposes.

[23] System interface 440 may be coupled to the rest of a system, such as a processor or VGA BIOS, allowing for communication between the graphics controller and the system, such as when a power supply switch occurs. Video interface 450 may be coupled to a monitor such as an LCD and may include both a VCLK video clock signal. Memory control interface 470 may be coupled to memory 480 and used to control and transfer information to and from memory 480. Memory control interface 470 may include a memory clock MCLK which may be used to synchronize signals with memory 480. Memory 480 need not be incorporated in the same physical package as graphics controller 400, provided that memory 480 is coupled to memory control interface 470. Power control interface 490 may be coupled to a power supply internal or external to the graphics controller 400, for purposes of controlling the power supply.

[24] Controller 460 is coupled to all of the previously mentioned components or blocks, and may be used to coordinate their operations to achieve performance of the graphics control operations. The components of graphics controller 400 may be implemented as portions of circuitry, such that 2D engine 410 may represent a first portion of circuitry for example. Note that 2D engine 410 and 3D engine 420 may be effectively turned off (powered down) depending on the modes of operation of the graphics controller, thus allowing for power savings.

[25] Turning to Figure 5, a graphics subsystem which may incorporate the invention is illustrated. Graphics BIOS 510 is the built in operating system of the graphics subsystem. It contains routines which may be used by graphics controller 520 and it may also be designed to effectively run an operating system on graphics controller 520 such that this operating system may monitor the data flowing to graphics controller 520. Graphics controller 520 receives and sends out graphics data 540 and video and graphics data 530. Video and graphics data 530 is sent and received by frame buffer 550. Graphics controller 520 also sends video data stream 560 which typically goes to the display system 580, such as a liquid crystal display or cathode ray tube display. Graphics data 540, in one embodiment, is the graphics data supplied from an underlying computer system attached to the graphics subsystem. It is this data which is monitored by the operating system running on graphics controller 520 to determine what resolution or what display mode is being utilized. Video and graphics data 530 is, in some circumstances, the actual data sent to the display. That data is translated from graphics data 540 by graphics controller 520. As a result video and graphics data 530 may or may not resemble graphics data 540 even though it effectively encodes the same image. It will be appreciated that in one embodiment of the invention the components illustrated in Figures 2 and 3 are incorporated within graphics controller 520 as registers and other logic within the processor that are subject to the control of routines from graphics BIOS 510 running on graphics controller 520.

[26] Turning to Figure 6, a system utilizing the invention is illustrated. Processor 610 is coupled to control hub 630. Control hub 630 is also coupled to graphics subsystem 620, to memory 640 and to system bus 660. Control hub 630 may be an AGP or PCI controller for example. Alternatively, control hub 630 may represent a combination of a north bridge and south bridge for example. System bus 660 is coupled to peripherals 650. Graphics subsystem 620 is also coupled to monitor 670. Graphics subsystem 620 may receive instructions and data from control hub 630. It may also request data from memory 640 through control hub 630 and likewise request interrupts to processor 610 through control hub 630 and request information or data from peripherals 650 through control hub 630 and system bus 660. Processor 610 may control memory 640, system bus 660 and peripherals 650 in graphics subsystem 620 and monitor 670 through control hub 630. In one embodiment graphics subsystem 620 incorporates all of the components illustrated in Figure 5 such as the graphics BIOS 510, graphics controller 520 and frame buffer 550. In that embodiment graphics data 540 is transmitted and received along the coupling between graphics subsystem 620 and control hub 630. Video data 560 is transmitted and received along the coupling between graphics subsystem 620 and monitor 670.

[27] Figure 7 illustrates another alternate embodiment of a system. Processor 710 is coupled to a bus 760, such as a PCI bus. Memory 720 is also coupled to the bus 760, as is graphics controller 730 and video controller 740.

Both video controller 740 and graphics controller 730 are coupled to LCD 750, a liquid crystal display.

[28] In the foregoing detailed description, the method and apparatus of the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the present invention. The present specification and figures are accordingly to be regarded as illustrative rather than restrictive.